WHAT IS CLAIMED IS:

1. An elastic store circuit which absorbs a propagation delay time difference among plural pieces of data, comprising:

a clock selector for selecting a read clock from a plurality of clocks corresponding to the data;

a data receipt detection circuit for detecting receipt of plural pieces of data;

a longest delay data detection circuit for detecting data having a longest propagation delay time; and

a reset circuit for receiving output from said longest delay data signal detection circuit and the read clock, and transmitting a reset signal to the data receipt detection circuit and a read address counter of elastic store memories.

2. The elastic store circuit according to claim 1, wherein said reset signal is transmitted to said data receipt detection circuit through the read address counter of the elastic store memories.

3. The elastic store circuit according to claim 1, wherein said data receipt detection circuit comprises a plurality of flip-flop circuits for receiving a frame pulse.

4. The elastic store circuit according to claim 3, wherein said flip-flop circuit is a set/reset flip-flop circuit, and a set terminal of the flip-flop circuit receives the frame

pulse, and a reset terminal of the flip-flop circuit receives the reset signal.

5. The elastic store circuit according to claim 1, wherein said longest delay data detection circuit is an AND circuit for receiving a plurality of output signals of said data receipt detection circuit.

6. The elastic store circuit according to claim 1, wherein said reset circuit comprises:

a flip-flop circuit for receiving the read clock; and

an AND circuit for outputting a reset signal upon receipt of a signal from the flip-flop circuit.

7. An elastic store circuit which absorbs a propagation delay time difference among plural pieces of data, comprising:

a clock selector for selecting a read clock from a plurality of clocks corresponding to the data;

a data receipt detection circuit comprising a plurality of flip-flop circuits for receiving a frame pulse;

a longest delay data detection circuit comprising an AND circuit for receiving each output signal of said flip-flop circuits;

a flip-flop circuit for receiving output of said longest delay data detection circuit and the read clock; and

a reset circuit comprising a read address counter of elastic store memory, and a two-input AND circuit for

transmitting a reset signal to said data receipt detection circuit.

8. A data receiving method, comprising the steps of:

receiving data through a plurality of transmission lines, and storing the data in corresponding elastic store memory;

receiving a plurality of clocks and frame pulses corresponding to the data;

selecting a read clock from the plurality of clocks;

receiving the frame pulses by an AND circuit, and detecting receipt of a latest data; and

reading data from each elastic store memory according to a reset signal based on output of the AND circuit and the read clock.